Abstract of the Disclosure:

A delay adjusting circuit that can minimize a delay at selectors even when the number of delay stages and the number of selector stages are increased, to enable a stable and speedy operation. As selectors S in a delay producing circuit (11), 2:1 selectors, each of the type that selectively outputs one from two inputs, may be used which are connected to input/output portions of N-stage delay elements D1 to DN for enabling delayed output of an even-stage delayed clock signal (Even) and an odd-stage delayed clock signal (Odd). In this case, the 2:1 selectors are arranged in a two-stage configuration including the for-even-stage selectors (S1, S3, ···, Sn, S(n+2)) and the for-odd-stage selectors (S2, ···, S(n+1), S(n+3)). The even-stage delayed clock signal (Even) is obtained through the first-stage selector S1. The odd-stage delayed clock signal (Odd) is obtained through the second-stage selector S2.